ISSN 1392-2114 ULTRAGARSAS (ULTRASOUND), Vol. 65, No. 4, 2010.

Analysis of the digital signal processing influence on time-of-flight estimation

L. Svilainis, S. Kitov

Signal processing department, Kaunas University o f Technology,
Studentu str. 50, LT-51368 Kaunas, Lithuania, tel. +370 37 300532,
E-mail:linas.svilainis@ktu.lt

Abstract

Application of digital filters in ultrasonic data acquisition system has been investigated. The work analyses the digital signal processing influence on a time of flight (*TOF*) estimation when applied on ultrasonic signals. The *ToF* estimation was done using the direct correlation technique of the sampled signal. The subsample estimation was done using parabolic interpolation of discrete direct correlation. The investigation covers the ADC and digital filter rounding noise influence on amplitude and *TOF* estimation performance. The theoretical equations for interpolation-influenced and quantization-influenced random errors assessment have been suggested. The acquisition system has been developed, including Xilinx Spartan 3E Field programmable gate array (FPGA), high speed 10 bit ADC and USB2 high speed interface. FPGA fixed point FIR filters have been developed and implemented. AccelDSP development suit was used to create the filters simulation environment in MATLAB.

Numerical simulation was used to analyze the filtering performance, influence of electronics noise, rounding errors and interpolation errors on *TOF*. Experimental results are documented and presented in tables and figures. It has been concluded that a digital filter output has to be quantized according to the processing gain obtained; otherwise rounding noise is increased, causing the *TOF* estimation to degrade.

Keywords: Ultrasonic measurements, time-of-flight estimation, interpolation, digital signal processing, field programmable gate array.

Introduction

Ultrasound application for non-destructive testing and evaluation is very popular: this is the only method offering direct interaction with test media [5, 6, 9]. Application in hard to access areas is demanding smaller equipment size [7, 8]. Ultrasound equipment should contain filters for recovery after excitation pulse, radial oscillations of ultrasonic transducer reduction electronics, noise reduction and EMI reduction [14] filters. But applications using the time domain need the stability of a group delay of filtering stages. Digital signal processing seems an attractive approach: signal filtering take as little space as field programmable gate array (FPGA) [10, 11] chip which is included in system topography anyway for analog-to-digit converter (ADC), buffer memory control and other acquisition purposes [12-14]; the filter stability is defined by a clocking oscillator (usually 50-100 ppm); high filter orders can be attained; flexibility of filter configuration.

Application of real time digital filters in ultrasonic data acquisition system was investigated (both programmable logic (CPLD/FPGA) both implemented in PC). The investigation will cover filter rounding noise and AC response performance.

The processing gain

Signal amplitude and phase estimation is an easy task if no noise is present. But the conditions, when the signal is corrupted by an additive white Gaussian noise, are unavoidable in reality. Then the amplitude and phase estimation becomes a more difficult task. Sine fitting using least squares error technique [1], Fourier transform [2], interpolated discrete Fourier transform (IpDFT) [3], wavelet transform [4], sine wave correlation (SWC) [18] etc. are used for a parameter estimation. In all the cases mentioned there is a certain improvement over instantaneous signal-to-noise ratio (SNR) after processing. This improvement can be addressed as a processing gain [16, 17]. This gain is obtained because the noise after ADC acquisition is spread in the first Nyquist zone producing a certain noise power density N_0:

$$N_0 = \frac{U_N^2}{f_N} = \frac{2U_N^2}{f_s}, \quad (1)$$

where U_N is the noise root mean square (RMS) value and f_s is the signal sampling frequency. The digital signal processing usually involves the bandwidth reduction to some bandwidth B, which in most cases can be obtained from the signal sample length t_{signal} in the time domain or the number of samples taken M with the sampling period T_s.

$$B = \frac{1}{t_{signal}} = \frac{1}{T_s M} = \frac{f_s}{M}. \quad (2)$$

Then noise with the noise power density N_0 will produce smaller RMS (U_{Nproc}) in the time domain due to the narrower B:

$$U_{Nproc}^2 = \frac{2U_N^2}{f_s} \cdot B = \frac{2U_N^2}{f_s} \cdot \frac{f_s}{M} = U_N^2 \frac{2}{M_s}. \quad (3)$$

The processing gain is usually indicated as the ratio of acquisition bandwidth and the processing bandwidth [16], but in our case it can be related to the signal record length expressed as a square root of samples $M/2$ (see Eq. 3 and [15]). Two main noise sources can be considered: i) electronics noise, contributed by the signal source thermal noise and amplifier stages voltage and current noise [19]; and ii) quantization noise [16]:

$$U_{ADCnRMS} = \frac{U_{REF}}{2^K \sqrt{12}}, \quad (4)$$

where K is the ADC bits number, U_{REF} is the ADC range, usually defined by a reference voltage.

Time of flight estimation

One of the most common tasks in ultrasonic systems is to define the time-of-flight (*ToF*) of the ultrasonic signal. In most common case the maximum of the matched filter output is used as the *ToF* estimate. The minimal random errors produced can be evaluated using the Cramer-Rao lower bound (CRLB). [20,21]:

$$\sigma(TOF) \geq \frac{1}{2\pi F_e \sqrt{\frac{2E}{N_0}}}, \quad (5)$$

where E is the signal energy, F_e is the effective bandwidth of the signal. The signal $s_T(t)$ energy can be calculated either using signal temporal presentation or signal spectral density (SSD) $S(f)$:

$$E = \int_{-\infty}^{\infty} |s_T(t)|^2 dt = 2\int_0^{\infty} S(f) \cdot S^*(f) df . \quad (6)$$

The effective bandwidth of the ultrasonic RF signal can be calculated as:

$$F_e^2 = \frac{\int_{-\infty}^{\infty} (f - f_0)^2 |S(f)|^2 df}{E} + \frac{\left[\int_{-\infty}^{\infty} f |S(f)|^2 df\right]^2}{E^2}. \quad (7)$$

The case above is the analytical expression. Digital signal processing introduces the quantization and sampling errors [22]. The application of the sampling frequency following the Nyquist criteria ensures that the subsample values can be obtained using the *sinc* function. At peak position (Fig.1), a parabolic interpolation is sufficient [23].

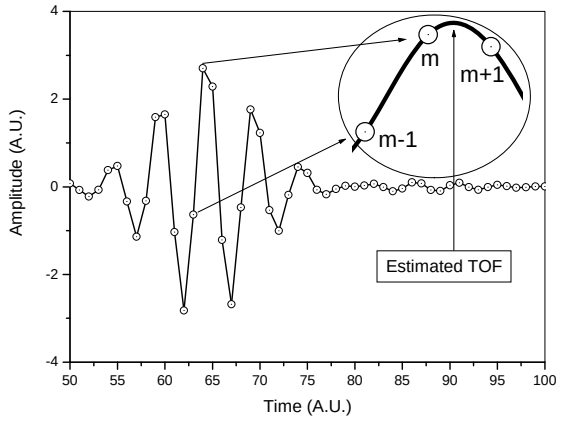

Fig. 1. **Parabolic interpolation for TOF estimation [23]**

The peak positions m-1, m and m+1 can be used directly to find the parabolic equation for apex and the *ToF* value obtained directly:

$$ToF_{\#P} = \frac{1}{2} \frac{(y_{m-1} - y_{m+1})T_s}{y_{m-1} - 2y_m + y_{m+1}} . \quad (8)$$

The Eq. 8 can be used to calculate the additional *ToF* subsample estimation errors introduced due to the noise present on the sampled points:

$$\sigma_{\#p}(ToF) = T_s \frac{N_0}{E} \frac{\sqrt{\left(2y_m^2 + y_{m-1}^2 - 2y_{m-1}y_{m+1} + y_{m+1}^2\right)}}{(y_{m-1} - 2y_m + y_{m+1})^2} . \quad (9)$$

A similar exercise was presented in [23]. But what if the signal is filtered first and then transferred for further processing via certain resolution digital communication channel?

The experimental system for digital signal processing

The acquisition and processing system (Fig. 2) has been developed, based on Xilinx Spartan 3E FPGA, high speed 10 bit ADC AD9215 and USB2 high speed interface CY7C68013. Fig. 2 presents the designed hardware setup, including operational amplifier for a single-ended to differential conversion, anti-aliasing filter, analog-to-digital converter (ADC), SDRAM for temporary data storage and the high speed USB bridge.

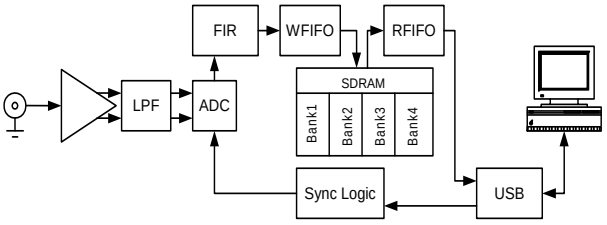

Fig. 2. **The experimental system structure (hardware setup)**

The core of the system is the Spartan3E Starter Board [24] from Digilent Inc. It features a 500K gate Spartan 3E XC3S500E FPGA, 32MB Micron MT46V32M16 double data rate (DDR) synchronous 8Mx16x4bank dynamic random access memory (SDRAM) and other supporting circuitry, while analog circuitry and the USB bridge are mounted on a daughter board.

The daughter board contains coaxial connectors for analog signals input, single-ended to differential signal converter, differential amplifier, anti-aliasing filter, high speed 10 bit ADC and USB2 high speed interface IC from Cypress.

The sampled data are sent via USB communication channel to a host personal computer (PC), where it can be analyzed both statistically and in the time domain. The digital filter under investigation is in between the analog to digital converter and the temporary data storage. The temporary data storage is a 8Mx16x4bank SDRAM, controlled by the FPGA firmware to implement First In, First Out (FIFO) logic. Such approach allows to have a flexible length, maximum 32M samples FIFO.

Filters

The digital signal filtering using a finite impulse response (FIR) can be presented as a convolution of the incoming signal s_i with the digitally represented filter impulse response a_i:

$$C_{out} = \sum_{i=0}^{N} a_i \cdot C\left(Z^{-i}\right). \quad (10)$$

For implementation, we have used a direct-form pipelined FIR filter implemented as a systolic multiply-accumulate architecture depicted in Fig. 3.

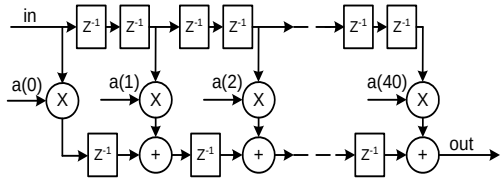

Fig. 3. **Filter configuration used**

In this architecture every tap of the delay line is multiplied by a corresponding coefficient and registered by a memory element, resulting in a short signal propagation path, witch leads to high filter throughput.

FPGA fixed point FIR filters have been developed and implemented in VHDL hardware description language. AccelDSP development suit was used to create the filters simulation environment in MATLAB.

The digital filters were implemented in FPGA and testing signals acquired using acquisition system developed. The filter AC response was measured passing the chirp signal through a filter. Refer Fig. 4 for signal magnitude spectrum used for testing.

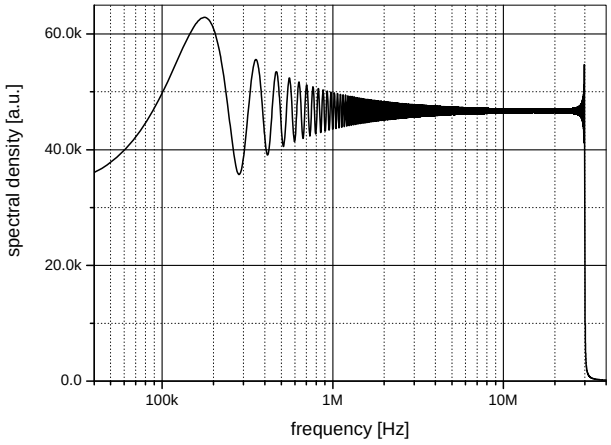

Fig. 4. **Test signal spectrum**

Using the spectra of the signal supplied to filter and at the filter output filter AC response was obtained:

$$T_{filt}(j\omega) = \frac{S_{out}(j\omega)}{S_{in}(j\omega)}. \qquad (11)$$

AC response for 40 taps FIR equiripple and least squares filters are presented in Fig. 5. Note the difference in filter gain though taps number is the same. This means that the resolution required to store the filtering result will differ.

The filter cutoff frequency was 5 MHz and the stopband frequency was 9 MHz with the stopband attenuation 64 dB (demanded by 10 bit decimation from 100 Ms/s to 10 Ms/s). Another filter (Fig. 5) had the same cut-off frequency and stopband frequencies and attenuation but was designed by a least squares filter design methodology. Implementing the designed filter in hardware resulted in FPGA resource utilization, described in Table 1.

The placement of filter logic on FPGA die is presented in Fig. 6. It can be seen that logic mapping is efficient in terms of area and available logic utilization ratio. Highly optimized FPGA fabric routing results in short propagation paths, witch are crucial for filter throughoutput, especially for complex filters involving large amount of logic resources.

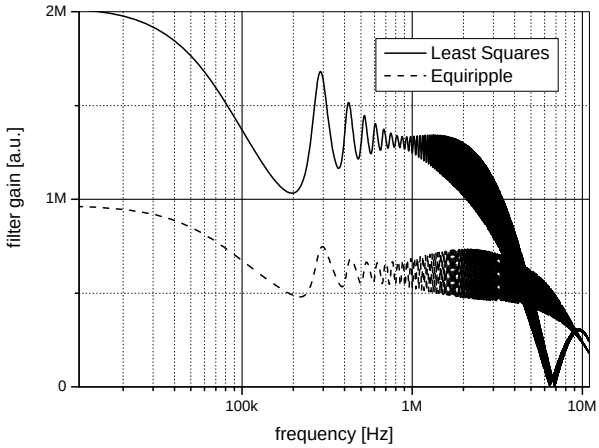

Fig. 5. **FIR filters AC response**

Table 1. **FPGA resource utilization summary**

Logic resource	Used	Available
Number of Slice Flip Flops	790 (8%)	9,312
Number of 4 input LUTs	556 (5%)	9,312
Number of occupied Slices	540 (11%)	4,656
Total Number of 4 input LUTs	556(5%)	9,312
Number of RAMB16s	1 (5%)	20

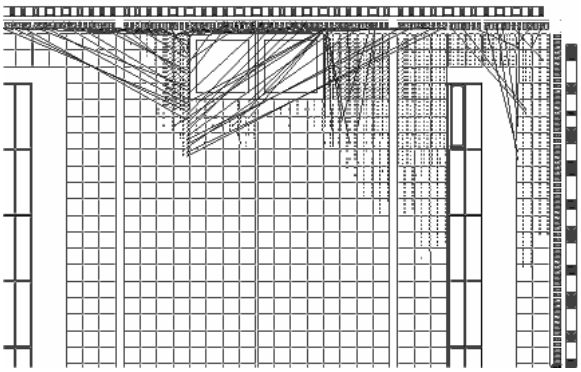

Fig. 6. **Filter logic placement on FPGA die**

The FPGA used provides the basic hardware for signal processing tasks. That is, multiply-and-accumulate, multiply-and-store or pre-adder have to be implemented "manually", using the basic logic. Even at such case the resources used are only small fraction of those available on a chip. The FPGA's that are dedicated for signal processing are enriched with hardwired digital signal processing blocks, such as the Xilinx DSP48 DSP slice which has the aforementioned blocks implemented in silicon. This means that plenty of processing tasks can be

assigned to FPGA without even notable increase in the resources used. Due to several reasons processing in FPGA is performed using a fixed point. Our aim was to investigate what are the pitfalls of embedded digital signal processing using fixed point arithmetic's.

Experimental investigation

Apart from the real-world experiment, a numerical simulation has been carried out in MATLAB environment. The sine wave correlation (SWC) technique has been implemented for a measured signal amplitude and phase estimation. Experiments were repeated 5000 times and the amplitude standard deviation obtained. Three cases were investigated on 1 MHz CW signal, result stored on 8k memory:

1. Using 100 MHz sampling frequency and 10 bit ADC with anti-aliasing filter;
2. Using 100 Ms/s sampling frequency and 10 bit ADC with preceding anti-aliasing filter, but then was decimated to 10 Ms/s with anti-aliasing filter during decimation and stored as 10 bit.
3. Using 10 Ms/s sampling frequency, 10 bit ADC with preceding anti-aliasing filter.

Experiments were carried out in MATLAB. The system input noise density was varied. The recorded signal was processed using SWC and the obtained magnitude (5000 records) was used to produce experimental standard deviation and mean. The results when quantization error (no ADC present-floating point data) was not taken into account are presented in Fig. 7.

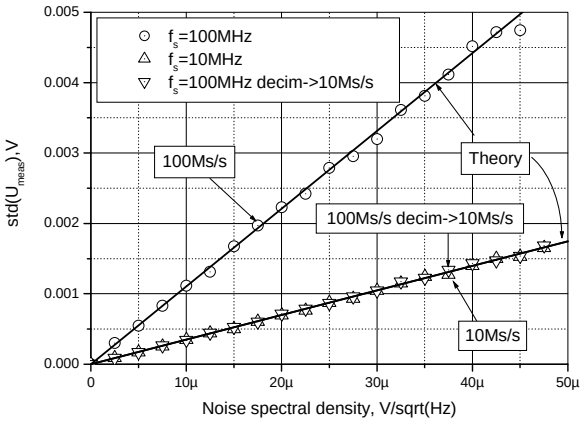

Fig. 7. **Voltage standard deviation vs. noise spectral density**

Theoretical prediction used Eq. 3. As it was explained above (based on Eq. 3), only the filter bandwidth is influencing the processing gain. Then, keeping the record length 8 k, gives the same filter bandwidth for the 10 Ms/s cases and a wider bandwidth for the 100 Ms/s case.

It was concluded that a high sampling frequency is of no advantage: much larger sample length is needed to maintain the same accuracy as with much smaller sampling frequency. The experiment adhered well with the prediction of Eq. 3. Is use of 100 Ms/s is unavoidable, decimation to a lower frequency can be done using the same FPGA: there is plenty of chip space left. It should be noted that decimation used to produce Fig.7 results was using anti-aliasing filter to remove the excessive noise from the frequency range which will be aliasing after decimation.

When quantization was applied, the carrier frequency was varied and kept as a fractional number of the sampling frequency; a small amount (10 nV/sqrt(Hz)) of electronics noise was injected to simulate the real case. This was done to ensure the quantization errors are not periodic and are equally spread over frequency band. The results are presented in Fig. 8.

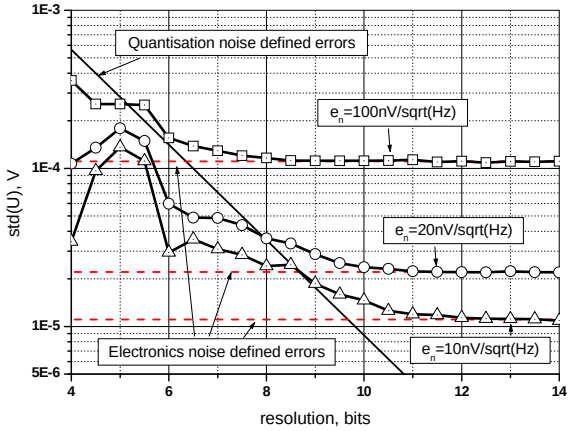

Fig. 8. **Amplitude estimation errors vs. ADC resolution**

ADC resolution was varied from 4 to 16 bits. It was concluded that the quantization noise should match the electronics noise: otherwise noise statistics is distorted. There is no need for ADC resolution increase beyond the limit defined by electronics RMS noise level, since the electronic noise starts to dominate; but ADC resolution can be reduced beyond: the processing gain will be nonlinear, there will be an increase of systematic errors.

Influence of digital signal processing on temporal parameters variance was investigated. A pulsed system operation was assumed, the *ToF* estimation was used as the pulse arrival time. The structure of the numerical simulation is depicted in Fig. 9.

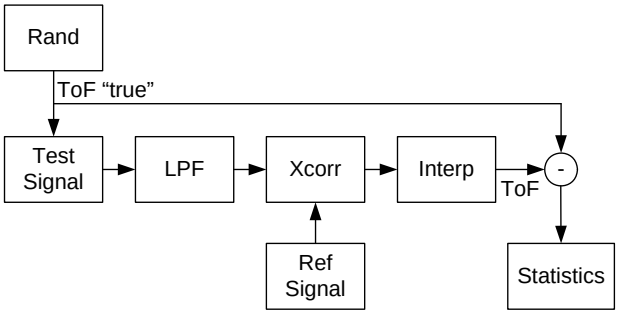

Fig. 9. **TOF numerical simulation experiment structure**

During the experiment, a sine wave with the Gaussian envelope was generated with a random (uniform distribution) shift in the time ("true" *ToF*) that is varied within a sampling period. The generated test signal is later passed to the digital low-pass filter. The filtered signal is correlated with a reference signal (also filtered) and the

peak of the correlation is approximated by the second order polynomial using Eq. 9 to obtain the *ToF* estimate. An absolute error of the time-of-flight is obtained by subtracting the "true" *ToF* value from *ToF* estimate. The result is stored for statistical analysis: standard deviation and mean value are obtained after 20000 iterations have been reached. *ToF* randomization was introduced to avoid the quantization influence on the *ToF*: experiment presented in [22] indicated that *ToF* errors lag plot turns discrete if the quantization noise starts prevailing.

The aim was to decide what will be the influence of a digital filter application, what resolution should be used to store the digital fixed point filter output. The same AC response filter was used (Fig. 10).

Six conditions were investigated:

1. The signal was sampled and quantized using the variable resolution ADC; ADC resolution was varied from 6 to 24 bits;
2. The signal was sampled and quantized using the variable resolution ADC; the reference signal was filtered by filter Fig. 10;
3. The signal was sampled and quantized using the variable resolution ADC; then converted to a floating point number, filtered (see Fig. 10 for filter AC response) and the result was left floating point;
4. The signal was sampled and quantized using the variable resolution ADC; then processed with the same resolution output bus filter;
5. The signal was sampled and quantized using the fixed, 9 bit resolution ADC; then processed with a variable resolution output bus filter; the resolution was varied from 6 to 24 bits;

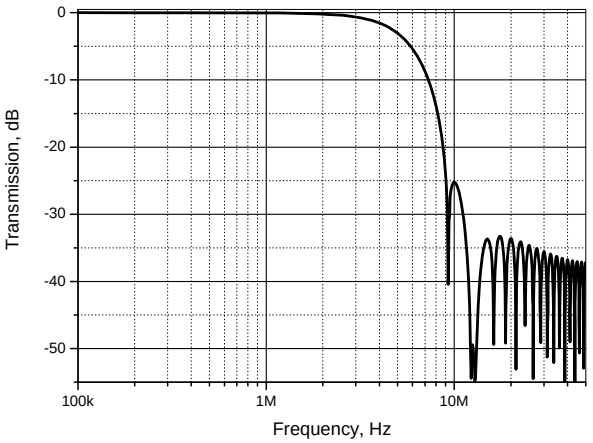

Fig. 10. **Filter AC response**

The standard deviation after 20000 iterations was obtained and results presented in Fig. 11.

It was concluded that application of the filter slightly improves that ToF random errors performance. The same result is achieved if the reference signal is filtered. Since filtering both the reference and the incoming signal is the double filter application, in order to achieve the same results the reference signal has to be filtered twice if no filtering is planned. In real world applications the reference signal filtering will occur naturally. It was concluded that filtering does not improve the signal performance if succeeding matched filtering is used. This is because the matched filter is taking only the bandwidth present in the reference signal. The removal of frequency components beyond the reach of the matched filter does not influence the result. If filtering is used, keeping filter output resolution the same as input will degrade the performance by roughly square root of two. This is because the filter is giving the processing gain thanks to which noise standard deviation in the time domain is reduced. If this gain is not addressed by the increased filter output bus resolution the noise power density is increased.

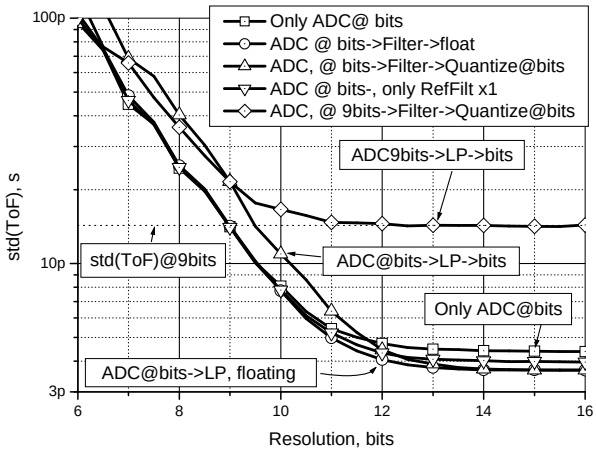

Fig. 11. **TOF variance vs. ADC and filter output resolution**

The ratio of acquisition bandwidth and processing bandwidth is used to calculate [16] the processing gain. Logarithm of power two of this defines the number of bits to be added. In our experiment we used 100 Ms/s which corresponds to the 50 MHz Nyquist bandwidth. Application of 5 MHz LP filter gives the processing gain of 10, what corresponds to 3 additional bits. Closer investigation of Fig.11 reveals that in the case of 9 bit ADC followed by filter only at 11 bits filter output bus resolution random errors are back to the level corresponding to 9 bits without filtering (note the label std(*ToF*)@9bits).

Conclusions

Though digital signal processing is a stable and flexible tool for signal performance improvement, effects of filter application should be carefully considered. Investigation results indicate that a digital filter output has to be quantized according to the processing gain obtained; otherwise rounding noise is increased, causing the *TOF* estimation to degrade.

Acknowledgement

This work was partly supported by the Lithuanian Science Council Student Research Fellowship Award.

References

1. **Silva M., Ramos P.M. et.al.** A new four parameter sine fitting procedure, Measurement. 2004. Vol. 35(2). P.131-137.

2. **Yang J. Z., Liu C. W.** A precise calculation of power system frequency, IEEE Power Engineering Review, TPD. 2001. Vol..16(3). P.361-366.
3. **Borkowski J.** LIDFT—The DFT Linear Interpolation Method IEEE Transactions on Instrumentation and Measurement. TIM. 2000. Vol. 49(4).P.741-745.
4. **Kuang W. T., Morris A. S.** Using short-time Fourier transform and wavelet packet filter banks for improved frequency measurement in a Doppler robot tracking system, IEEE Transactions on Instrumentation and Measurement. TIM 2002., Vol. 51 (3). P. 440-444.
5. **Kažys R., Raišutis R., Žukauskas E., Mažeika L. and Vladišauskas A.** Air-coupled ultrasonic testing of CFRP rods by means of guided waves, International Congress on Ultrasonics. Physics Procedia. 2010. Vol. 3(1). P. 185-192.
6. **Pallav P., Hutchins D. A., Gan T. H** Air-coupled ultrasonic evaluation of food materials. Ultrasonics. 2009. Vol. 49. P. 244–253.
7. **Athanasopoulos G. I., Carey S. J., Hatfield J. V.** A high voltage pulser ASIC for driving high frequency ultrasonic arrays. IEEE Ultrasonics Symposium. 2004. 2 P.1398 – 1400.
8. **Johansson J., Delsing J.,** Microelectronics mounted on a piezoelectric transducer: Method, simulations, and measurements, Ultrasonics. 2006. Vol. 44. P. 1–11.
9. **Tangel A., Yakut M., Afacan E., Guvenc U., Sengul H.** An FPGA-based multiple-output PWM pulse generator for ultrasonic cleaning machines, IEEE Conference on Applied Electronics. 2010. P.1 – 4.
10. **Engy R.EL Mahdy, et al.** FPGA Based Backend System for Medical B-Mode Ultrasound Imaging, Proc. Cairo biomedical engineering conference. 2006. P.1-4.
11. **Aitken M.** FPGA-Based Data Acquistion System for Ultrasound Tomography. Project report, Department of Electrical Engineering, University of Cape Town. 2006.
12. **Hu Ch. H., Zhou Q., Shung K .K.** Design and Implementation of High Frequency Ultrasound Pulsed-Wave Doppler Using FPGA. IEEE Trans. Ultrason. Ferroelectr. Freq. Control. 2008. Vol. 55(9). P.2109–2111.
13. **Zurek P.** Implementing FPGA technology in ultrasound diagnostic device. IEEE proc. Conference on Information Technology and Applications in Biomedicine. 2008. P.179 – 182.
14. **Fritsch C., Giacchetta R., Gonzalez R., et al.** A Full Featured Ultrasound NDE System in a Standard FPGA. ECNDT Proceedings 2006. P.1-10.
15. **Svilainis L., Dumbrava V.** Amplitude and phase measurement in acquisition systems. Matavimai. 2006. Vol. 38. P. 21-25.
16. **Kestler W. (editor).** Analog-digital conversion. Analog devices. 2004.
17. IEEE Standard for Digitizing Waveform Recorders, IEEE Std 1057-2007. IEEE. 2008.
18. **Svilainis L., Dumbrava V.** Measurement of complex impedance of ultrasonic transducers. Ultragarsas. Vol.1(62). 2007. P. 26-29.
19. **Svilainis L., Dumbrava V.** Investigation of a preamplifier noise in a pulse-echo mode. Ultragarsas. Vol.3(56), 2005, P. 26-29.
20. **Rao C.** Information and the accuracy attainable in the estimation of statistical parameters. Bulletin of Calcutta Mathematics Society. Vol. 37. 1945. P. 81–89.
21. **Cramer H.** Mathematical Methods of Statistics. Princeton, NJ: Princeton Univ. Press. 1946.
22. **Svilainis L., Dumbrava V.** The time – of - flight estimation accuracy versus digitization parameters. Ultragarsas. 2008. Vol. 63(1). P.12-17.
23. **Svilainis L., Dumbrava V.** Analysis of the interpolation techniques for time – of - flight estimation. Ultragarsas. 2008. Vol. 63(4). P. 25-29.
24. Spartan 3E Starter Board, Digilent, Inc. 2010: http://www.digilentinc.com/Products.

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Skaitmeninio signalo apdorojimo įtakos sklidimo laiko įverčiui analizė

Reziumė

Nagrinėjamas skaitmeninių filtrų taikymas ultragarsiniam signalui, tiksliau - signalo amplitudės ir sklidimo laiko įverčių vidutinio kvadratinio nuokrypio priklausomybė nuo apdorojimo. Diskretizuoto ir kvantuoto signalo sklidimo laiko įverčiui gauti buvo taikomas tiesioginės koreliacijos metodas. Sklidimo laikui patikslinti tarp išrankų buvo naudojama pikinės srities interpoliacija, kartu ir parabolė. Tyrimo tikslas buvo įvertinti skaitmeninio analogo keitiklio ir skaitmeninio filtro kvantavimo ir apvalinimo paklaidų įtaką. Pasiūlytos teorinės analitinės išraiškos signalo vėlinimo laiko įverčio interpoliacijos atsitiktinėms paklaidoms, taip pat išraiškos kvantavimo paklaidoms įvertinti. Suprojektuota ir pagaminta duomenų surinkimo sistema, sudaryta iš Xilinx Spartan 3E programuojamo loginių ventilių lauko (FPGA) sparčiojo dešimties bitų skaitmeninio analogo keitiklio ir USB2 didelio greičio sąsajos. Maketo pagrindu sukonstruoti ir jame realizuoti fiksuotoj kablelio baigtinės impulsinės reakcijos (FIR) filtrai. Naudojantis AccelDSP projektavimo paketu sukurta filtrų emaliavimo MATLAB aplinkoje terpė.

Atlikti skaitiniai eksperimentai filtravimo kokybei, taip pat elektronikos ir apvalinimo triukšmų ir interpoliacijos įtakai, kuri reiškiasi nustatant sklidimo laiką, įvertinti. Eksperimento rezultatai parodyti lentelėse ir grafikuose. Nustatyta, kad skaitmeninio filtro rezultatą pakanka saugoti skyra, kurią sąlygoja apdorojimo stiprinimas; jeigu kvantavimo skyra bloginama, sklidimo laiko įvertis blogėja.

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