Exploration of DSP architectures in ultrasonic measurement applications

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Introduction

Number of ultrasonic measurement (UM) applications is increasingly growing. The most important ones are nondestructive testing of materials, sonar, distance and velocity measurements, medical applications. Many modern UM applications are based on digital signal processing (DSP) technologies that have been extensively developed during the last decade. Signal processing, e.g. filtering, correlation, averaging, improves signal-to-noise ratio and accuracy of measurements. However, DSP architecture comprises a significant, sometimes the major part of UM system hardware and cost. Also it sets certain restrictions on measurement speed and the expected signal-to-noise ratio. Therefore, rapid exploration and selection of rational DSP architectures are important issues in UM system design.

This paper describes a concept of DSP architecture exploration in UM applications. It suggests integrated model "UM application - DSP architecture" that allows to select the rational architecture following by the application requirements. The concept is illustrated with the correlation time delay estimation (TDE) task.

Part of DSP architecture in UM applications

The typical elements of an UM system are measurement object, signal generator, ultrasonic transducers and DSP architecture (Fig.1).

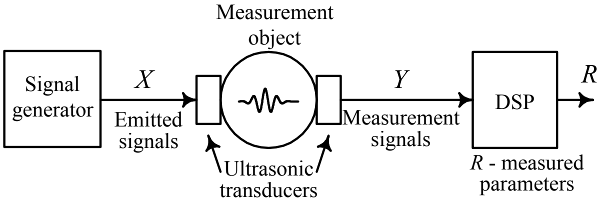


Fig. 1. **Typical elements of an UM system**

Characteristics of the whole system depend on the parameters of each element. The point is that the DSP architecture also makes influence into measurement characteristics. Therefore, it must be selected or designed according to the UM application requirements.

Various UM applications and systems have different characteristics. The common ones are signal-to-noise ratio SN_M, measurement time T_M and hardware resources C_M.

The DSP architecture Φ_{DSP} is an implementation of a certain function F_{DSP} (Fig.2). Broadly Φ_{DSP} can be characterized by processing error ε, processing time T and hardware resources C [1]. The architecture notion combines software structure, number format, internal structures of processing elements and a global structure of the system.

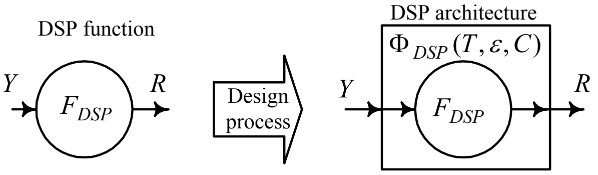


Fig. 2. **DSP function and its implementation architecture**

The same F_{DSP} can be implemented in a family of architectures with different values of ε, T and C:

$$\Phi_i = \Phi(\varepsilon_i, T_i, C_i). \qquad (1)$$

Characteristics of ε, T and C are closely related to each other. Increase of DSP speed means that more parallel hardware elements are needed. Reduction of ε requires larger number of bits and algorithms with more complex structures. Meanwhile, hardware resources increase system cost, power consumption, physical dimensions so they are subjected to a certain conceivable reduction.

In a particular application Φ_{DSP} must satisfy such formal restrictions [1]:

$$\varepsilon \le \varepsilon_0, T \le T_0, C \le C_0, \qquad (2)$$

where ε_0, T_0 and C_0 are bounds required by the application. Considering Φ_{DSP} in an UM application the restrictions (2) should be related with the application restrictions:

$$SN_M \le SN_{M0}, T_M \le T_{M0}, C_M \le C_{M0}. \qquad (3)$$

The latter ones are applied to the UM system as a whole. They concern all elements of the system, including DSP architecture. In order to select DSP architecture the parameters of other elements must be defined and fixed.

Characteristics of T and C often are easy predictable in DSP architectures. Basic DSP operations by nature have linear algorithms with fixed execution time. Values of T and C can be explicitly varied by using paralleling, pipelining and sequencing techniques [1], [12]. Moreover, a number of reusable DSP architectures, such as FIR filters, correlators, FFT processors recently are available with predefined T and C characteristics [13]. Therefore T and C will not discussed in this paper.

More complicated task is the prediction of the actual DSP error ε. Processing accuracy usually is characterised by a number format and wordlength. However, ε cannot be defined barely by these two parameters. It depends also on DSP algorithm structure and signal parameters. In some UM applications selection of DSP architecture with acceptable processing accuracy may be a problem. As the solution was proposed the model "UM application - DSP architecture". It should provide effective selection of rational DSP architectures.

Method of DSP architecture exploration

According to the method, DSP architecture exploration must be performed within the **model** (Fig. 3) which contains:

- Signal model $Y(P)$ with the parameter vector P ;
- DSP architecture model $\Phi_{DSP}(Q)$ with the parameter vector Q . Vector R^* is the measurement result evaluated by the Φ_{DSP} .

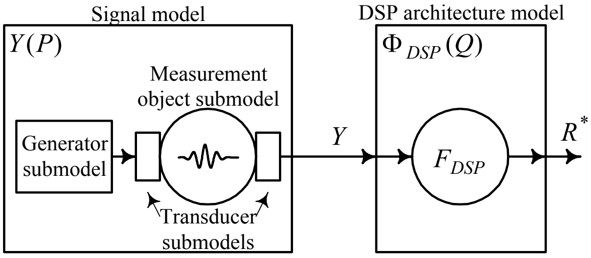


Fig. 3. **Model for DSP architecture exploration**

Furthermore $Y(P)$ can be a composed of generator, transducer and measurement object submodels. However, just signal and DSP architecture models were distinguished because two different designer specializations are necessary to manage them. Presumably, measurement object exploration, signal conditioning and selection of the DSP method lie within the competence of measurement engineers. Exploration, selection and prototyping of DSP architecture are better manageable by DSP design engineers.

The signal model in various UM tasks can be described by a number of parameters. One case of signal parametric description is given in the next section.

The DSP architecture model is shown in Fig. 4. It consists of signal digitization and processing submodels Φ_d and Φ_p . The architecture model is described by the parameter vector:

$$Q = \left\langle \Delta t_s, b_q, M, b_\Sigma, b_\Pi, b_e, b_d, b_B \right\rangle, \qquad (4)$$

where Δt_s - signal sampling period, b_q - quantization bit number, M - DSP algorithm description, b_Π - multiplier wordlength, b_Σ - accumulator wordlength, b_e - exponent wordlength, b_d - signal quantization wordlength, b_B - data bus wordlength.

Different values of these parameters bear corresponding errors $\varepsilon_d, \varepsilon_M, \varepsilon_\Pi, \varepsilon_\Sigma$ which degrade the measurement result R^*. The model helps to explore parameter-to-error relationships and select the appropriate parameter values.

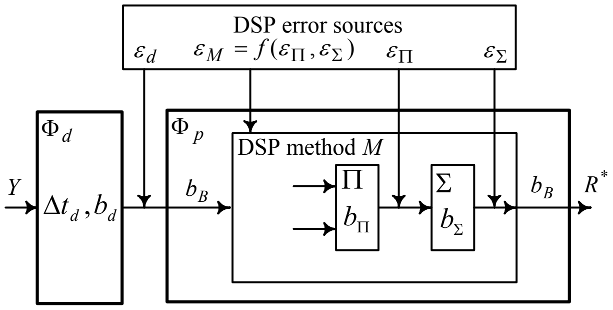


Fig. 4. **DSP architecture model**

The basic **implementation possibilities** of the model are hardware prototyping and software simulation. Hardware prototyping, in opposition to software simulation, affords to explore the architecture in real environment and real time, however, it is more expensive and less flexible. Practically, various combinations of both methods are used.

Recently a lot of prototypes and simulation tools is available. They manage different aspects within the UM system design. The following tool classes can be distinguished:

- Environments of system conceptual specification and modeling, such as Matlab, MathConnex, Ptolemy;
- UM prototypes that are dedicated for investigation of measurement object. They perform signal generation and registration. A notable example is Saphir system [6];
- Software for simulation of ultrasonic transducers, measurement object and signal propagation in it. Examples are Wave'2000 [14], UTSim [15];
- DSP prototypes that are preferable for real-time signal processing;
- Software for DSP architecture synthesis and simulation, e.g. processor simulators, tools for programmable gate array synthesis and simulation [13].

The method proposes a **software model** which integrates models of the UM application-specific signal and DSP architecture. This method points to place UM system model into single simulation environment, make it flexible and available to designers of the two mentioned categories.

This connective feature is not possessed by any of the above design tools. For example, DSP architecture design tools do not allow investigate how the SN_M depends on the number of bits. Ultrasonic simulation tools do not provide evaluation of how DSP error degrades the measurement result. Exploration of hardware prototype in real environment is expensive, few flexible and complicated due to many unknown parameters.

The applicable environment for the method implementation is MATLAB. It is well known for engineers as a tool of specification and conceptual modeling. A possible drawback of this software simulation approach is the need of powerful computer if the model becomes much detailed and complex.

Model in the case of correlation TDE task

Time delay estimation is the basic task in many UM applications. One of DSP methods commonly applied for TDE is the correlation method [5], [7], [11]. It points to find peaks of the correlation function (CCF) of the reference signal $x(t)$ and measurement signal $y(t)$. The CCF peaks with sufficiently large amplitudes are considered as time delay indicators. The DSP data-flow graph of this method contains digitization, CCF computation and peak detection functions F_d, F_{cf}, F_{pd}. They must be realized in a certain Φ_{DSP} (Fig 5).

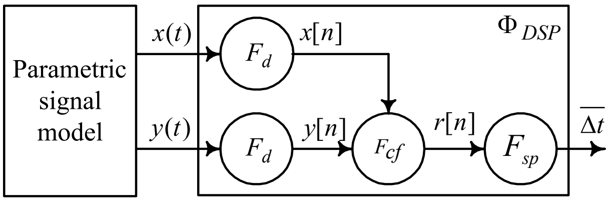


Fig. 5. **DSP graph for the correlational TDE task**

Signals. In this case the reference signal $x(t)$ is considered as energy impulse with defined duration T_p, amplitude A_p, center frequency v_0 and bandwidth Δv. Values of these parameters in a particular application would depend on excitation pulse duration, amplitude, transducer bandwidth and central frequency. A common mathematical model for such signals is the Gaussian radioimpulse [16] (Fig. 6). With a desirably small error it can be considered as a pulse of finite length and bandwidth.

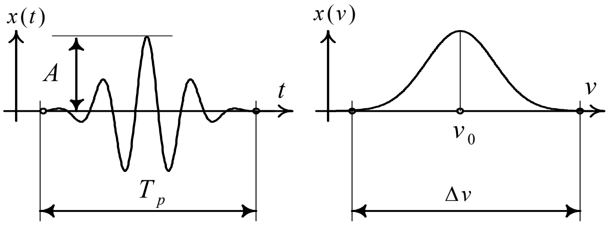


Fig. 6**. Signal parameters**

The measurement signal $y(t)$ is equal to the sum of K differently delayed and scaled $x(t)$ copies and random measurement noise $n(t)$:

$$y(t) = \sum_{i=1}^{K} A_i \cdot x(t - \Delta t_i) + n(t),\ t \in 0, T, \tag{5}$$

where $A_i \le 1$ and Δt_i are scale and delay of the i-th signal copy, T - time delay range. The CCF of $x(t)$ and $y(t)$ can be written as follows [5]:

$$r_{xy}(\tau) = \sum_{i=1}^{K} A_i \cdot r_{xx}(\tau - \Delta t_i) + r_{xn}, \tag{6}$$

where r_{xx} is autocorrelation function (ACF) of $x(t)$ and r_{xn} is the CCF noise. Infact, the DSP error is a constituent of this noise. For the simplicity in the experiments only this DSP-conditioned noise is considered.

The noise dependent **TDE characteristics** are sensitivity and uncertainty. Sensitivity is relative to signal-to-noise ratio which has the expression [5]:

$$SN_n = \frac{A_i \cdot r_{xx}(0)}{\sigma_n} = \frac{A_i}{\sigma_n}, \tag{7}$$

where σ_n is mean-squared and ACF-peak-normalised value of $n(t)$. Following [4], an ACF peak is detectable in the CCF if the following condition is satisfied:

$$A_i \ge \tfrac{1}{3}\sigma_n. \tag{8}$$

So, the sensitivity or minimal admissible signal-to-noise ratio corresponds to the equality sign set in (8).

Mean-square TDE uncertainty is equal [5]:

$$\sigma_{\Delta t} = \frac{0.93}{\pi \Delta v} \cdot \frac{A_i}{\sigma_n}. \tag{9}$$

Consequently, the signal model is described by the following collection of TDE task parameters:

$$P = \left\langle \Delta v, v_o, T_p, T, K, A[K], \Delta t[K], SN_{M0} \right\rangle, \tag{10}$$

where SN_{M0} is the required minimal signal-to-noise ratio and K, $A[K]$, $\Delta t[K]$ - the measurement object parameters.

Exploration example. In this case such signal parameter values were defined:

$$P = \left\langle \begin{matrix} \Delta v = 15KHz, v_o = 40KHz, T_p = 0.9ms, \\ T = 7ms, K = 3, A = [0.8;0.7;0.1], \\ \Delta t = [1.6ms;3.3ms;4.5ms], SN_{M0} = 40dB \end{matrix} \right\rangle . \tag{11}$$

The reference signal $x(t)$ here is a sequence of Gaussian pulses modulated by 13-element Barker code. The signal graphs are shown in Fig. 7.

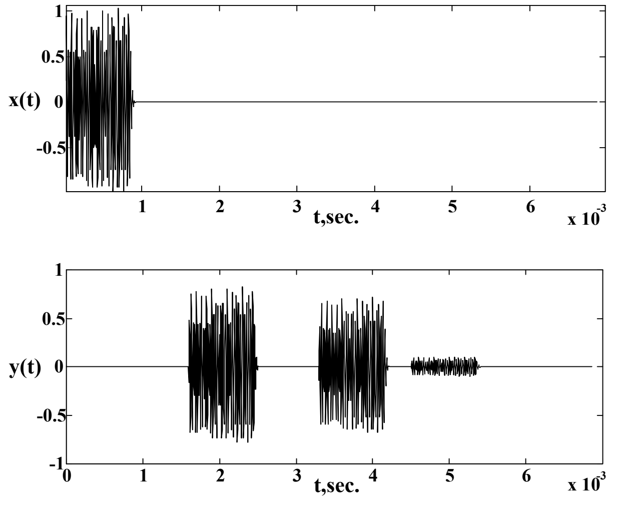


Fig. 7. **Signals** $x(t)$ **and** $y(t)$

The DSP architecture model was explored for several sets of Q. Firstly, sampling and quantization parameters were set. Sensitivity $SN_M = 40dB$ corresponds to $b_q = 8$

quantization bits [8]. The sampling frequency should be taken at least 4 times of signal highest frequency [8], so $\Delta t_s = 4\mu s$ was set.

Within the DSP architecture several CCF computation algorithms, data formats and wordlengths were used. One common algorithm is the direct algorithm [3] (here denoted by M1) which, likewise FIR filter, performs accumulation of many products. Another one is the fast algorithm M2 [3] based on fast Fourier transform (FFT):

$$\bar{r}_{xy} = IFFT\left[FFT(\bar{x})\cdot FFT(\bar{y})\right], \qquad (12)$$

where $\bar{x}$, $\bar{y}$, $\bar{r}_{xy}$ are the arrays of the signals and CCF. Also some signal-specific algorithms are applicable, e.g. the method for Barker coded pulse sequences [7]. The function F_{pd} only detects the CCF peaks and does not bear processing errors.

Figure 8 shows the CCF calculated by the MATLAB function *xcorr* that uses 64 bit floating-point arithmetic's. The CCF computed by M2 in 32 bit floating-point DSP architecture was not noticeably different from the one in MATLAB. However, in cases of longer signals and more complex DSP methods distortions can be larger.

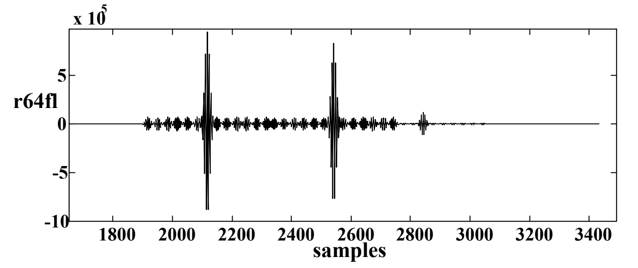
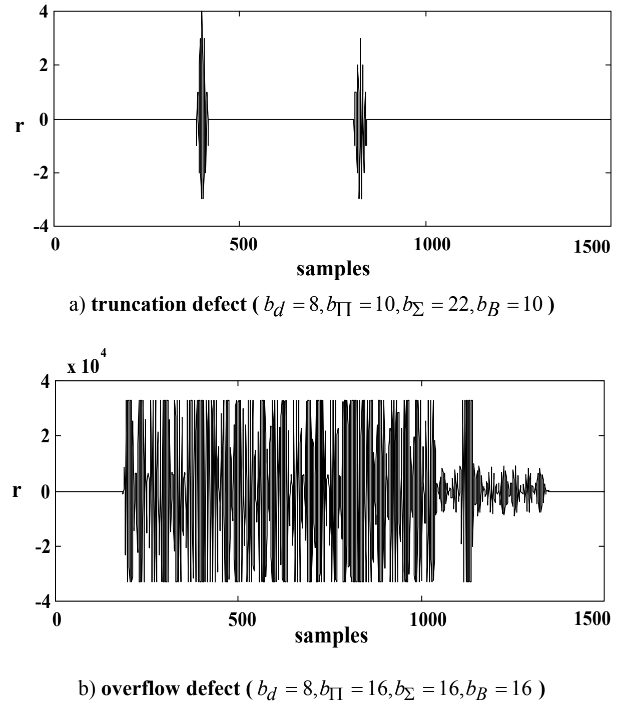


Fig. 8. **CCF computed by MATLAB (M2, floating-point, 64 bit)**

The DSP error grows reasonably faster in fixed-point architectures. Figures 9 and 10 present common CCF defects obtainable with the fixed-point arithmetic's.



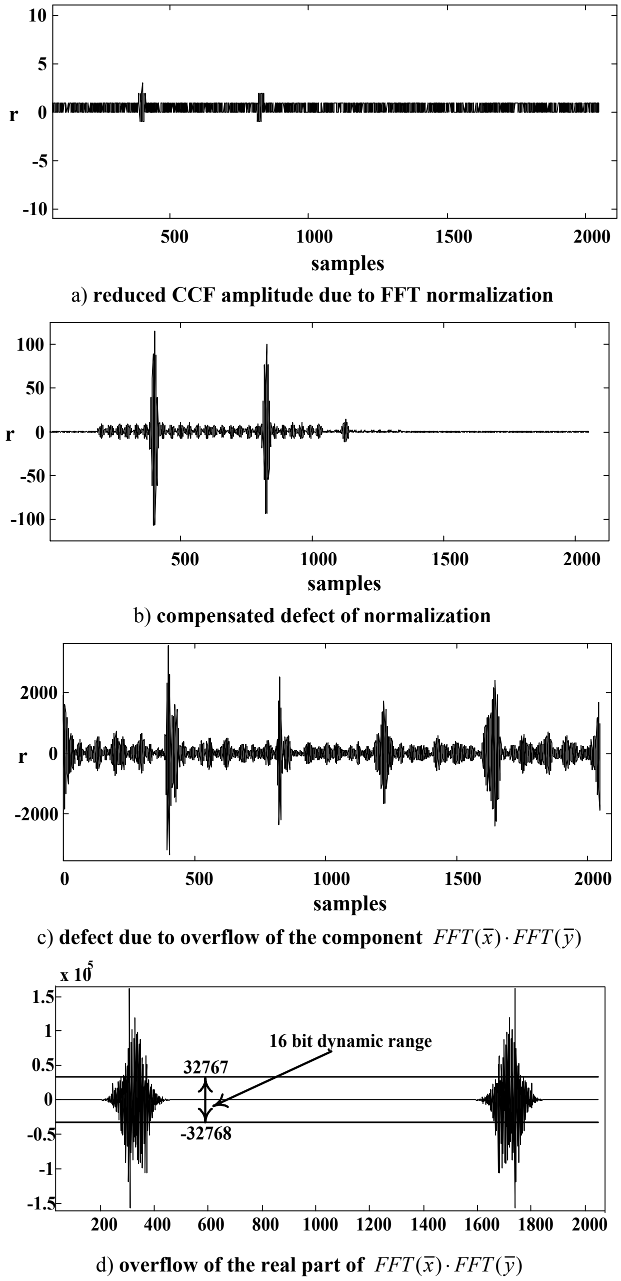
a) **truncation defect (** $b_d = 8, b_\Pi = 10, b_\Sigma = 22, b_B = 10$ **)**

b) **overflow defect (** $b_d = 8, b_\Pi = 16, b_\Sigma = 16, b_B = 16$ **)**

Fig. 9. **CCF defects (M1, fixed point)**

Figure 9 shows the CCF calculated by the direct method M1. Graph (a) illustrates that the small peak disappeared and became undetectable because the least significant bits were ignored or rounded within the multiplier and adder. Graph (b) shows the peak cutoff occur due to sum overflow.

Figure 10 shows the CCF calculated by the algorithm M2. The DSP error in M2 has a different character due to FFT computation specifics. Most of fixed-point FFT routines normalize FFT result by factor N, where N is the length of signal array [2]. Since M2 contains 3 FFT operations, the CCF normalization factor is equal to N^3, and for long signals the CCF amplitude is reduced enormously (Fig.10a). This defect can be partly compensated by multiplying the intermediate component $FFT(\bar{x})\cdot FFT(\bar{y})$ by some factor K (Fig. 10b). However, too large K will cause $FFT(\bar{x})\cdot FFT(\bar{y})$ overflow (Fig. 10d) and distortion of the CCF (Fig. 10c).



a) **reduced CCF amplitude due to FFT normalization**

b) **compensated defect of normalization**

c) **defect due to overflow of the component** $FFT(\bar{x})\cdot FFT(\bar{y})$

d) **overflow of the real part of** $FFT(\bar{x})\cdot FFT(\bar{y})$

Fig. 10. **CCF defects (M2, fixed point, 16 bit processor)**

Note, that the $FFT(\bar{x}) \cdot FFT(\bar{y})$ overflow depends on signal bandwidth $\Delta\nu$. For example, the energy of a white noise is gradually spread over the frequency range and hardly will reach the overflow. Meanwhile, the frequency spectrum of harmonic signals is shaped as a sharp and high peak that fastly tends to overflow cutoff.

Acknowledgement and conclusion

The method and model of DSP architecture exploration were suggested and applied in two scientific projects carried out at Ultrasound Research Institute and DSP Laboratory of Kaunas University of Technology. During these projects the ultrasonic vision system for mobile robot (project INCO-COPERNICUS No. ERB IC15-CT96-0726) [9], [10], [11], and high precision ultrasonic gas flowmeter have been designed. In both cases signal processing was necessary and the DSP architecture design presented a quite serious problem. The method proposed enabled solution of this problem.

The software model provides flexibility, it can be modified for different DSP methods, algorithms and signals. Therefore, the proposed method and model also are applicable for the design of other UM systems.

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Skaitmeninio signalų apdorojimo architektūrų tyrimas ultragarsinių matavimų uždaviniuose

Reziumė

Straipsnyje aprašytas metodas, leidžiantis efektyviau projektuoti ultragarsinio matavimo (UM) sistemas. Šiuolaikinėse UM sistemose aukštoms matavimo charakteristikoms pasiekti plačiai taikomas skaitmeninis signalų apdorojimas (SSA). Tačiau dažnai SSA architektūra sudaro didžiąją UM sistemos resursų dalį, taip pat mažina matavimo spartą ir signalo ir triukšmo santykis gali būti blogesnis negu tikėtasi. Metodas aprašo SSA paklaidų įtakos UM uždavinių charakteristikoms tyrimą naudojant modelį "Matavimo uždavinys - SSA architektūra" Šis modelis realizuojamas programiniu būdu. Metodui pademonstruoti buvo atliktas SSA architektūrų tyrimas signalų sklidimo trukmės įvertinimo koreliaciniu metodu uždavinyje.

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